

IN THE CLAIMS

1. (Currently amended) A nonvolatile semiconductor memory device comprising:
a ~~substrate;~~
~~a plurality of sectors on the substrate;~~
a sector on a substrate, the ~~each sector comprising including~~ memory cell transistors arranged in a cell array block and decoder transistors in a column decoder block;
wherein the transistors in the cell array block and column decoder block ~~in each sector~~ share a common bulk region, wherein the common bulk region is formed on the substrate and is connected to a bulk driver ~~provided in each of the sectors, each said~~ the bulk driver configured to commonly apply a bulk voltage to the common bulk region of the sector; and
wherein said semiconductor memory device is configured to electrically erase all the memory cell transistors in a the sector together.
2. (Original) A nonvolatile semiconductor memory device according to claim 1, wherein the semiconductor memory device is a NOR-type memory device.
3. (Original) A nonvolatile semiconductor memory device according to claim 1, further comprising a write driver and a sense amplifier.
4. (Original) A nonvolatile semiconductor memory device according to claim 3, wherein the write driver and sense amplifier are configured to be placed in a state of high impedance during an erase operation to avoid influencing circuit operation during the erase operation.
5. (Original) A sector structure of a nonvolatile semiconductor memory, said sector structure comprising:
a plurality of memory cell transistors arranged in a cell array block; and
a plurality of decoder transistors arranged in a column decoder block, wherein said memory cell transistors and decoder transistors are arranged on a common bulk region.
6. (Original) A sector structure of a nonvolatile semiconductor memory according to claim 5, wherein an erase operation is configured to erase all of the transistors in the sector simultaneously.

7. (Original) A sector structure of a nonvolatile semiconductor memory according to claim 5, said sector structure further comprising:
a plurality of word lines arranged in the cell array block, each word line being connected to a plurality of cell gates;
a plurality of bit lines arranged in the cell array block, each bit line being connected to a plurality of memory cell drains;
a plurality of common data lines connected to the bit lines;
a plurality of write drivers, each connected to a respective one of the common data lines; and
a plurality of sense amplifiers, each connected to a respective one of the common data lines.

8. (Original) A sector structure of a nonvolatile semiconductor memory according to claim 7, wherein each write driver and sense amplifier is configured to be placed in a state of high impedance during an erase operation.

9. (Original) A sector structure of a nonvolatile semiconductor memory according to claim 5, wherein said sector structure is configured to provide 64 Kbytes of memory.

10. (Currently amended) A sector of a nonvolatile semiconductor memory device ~~with a plurality of sectors, each sector~~ comprising:

a cell array block ~~comprising~~ including a plurality of word lines, a plurality of bit lines, and a plurality of memory cell transistors having gates and drains, each gate being connected to a corresponding word line out of the plurality of word lines, each drain being connected to a corresponding bit line out of the plurality of bit lines;

a source line driver commonly connected to a source of each of the plurality of memory cell transistors and configured to apply a source voltage;

a column decoder block comprising a plurality of column decoder transistors, each column decoder transistor connected to a corresponding bit line out of the plurality of bit lines and a common data line configured to select one bit line out of the plurality of bit lines; and

a common bulk region arranged in ~~each~~ the sector and formed immediately adjacent to a substrate region, wherein the plurality of memory cell transistors and the plurality of column decoder transistors in ~~each~~ the sector share the common bulk region; and

a bulk driver ~~provided in each of the sectors~~, each ~~said~~ the bulk driver configured to commonly apply a bulk voltage to the common bulk region of ~~that~~ the sector.

11. (Currently amended) ~~A nonvolatile semiconductor memory device according to claim~~ The sector of claim 10, wherein the nonvolatile semiconductor memory device is a NOR-type flash EEPROM.

12. (Currently amended) ~~A nonvolatile semiconductor memory device according to~~ The sector of claim 10, wherein the bulk region is a pocket P-well.

13. (Currently amended) ~~A nonvolatile semiconductor memory device according to~~ The sector of claim 10, further comprising a plurality of write drivers and sense amplifiers, a write driver and a sense amplifier, wherein each the common data line is connected to a corresponding one of the write drivers and a corresponding one of the sense amplifiers. the write driver and the sense amplifier.

14. (Currently amended) ~~A nonvolatile semiconductor memory device according to~~ The sector of claim 13, wherein the write ~~drivers~~ driver and the sense ~~amplifiers are each~~ amplifier configured to be placed in a state of high impedance during an erase operation.

15. (Currently amended) A nonvolatile semiconductor memory device comprising:

a substrate;

a ~~plurality of sector units, each unit, the~~ sector unit ~~comprising including~~ a common bulk region, the bulk region being formed on the substrate and connected to a bulk driver, ~~and wherein each~~ the sector unit is configured to be electrically erasable in response to an erase signal; and a plurality of memory cell transistors and transistors of a column decoder arranged in the common bulk region of ~~each~~ the sector unit and configured to commonly receive a bulk voltage.

16. (Currently amended) A nonvolatile semiconductor memory device according to claim 15, wherein ~~each~~ the sector unit further comprises a bulk driver configured to supply a bulk voltage to the common bulk region.

17. (Original) A nonvolatile semiconductor memory device according to claim 15, wherein said plurality of memory cell transistors are arranged in a cell array block, wherein said plurality of column decoder transistors are arranged in a column decoder block, and wherein said cell array block and said column decoder block are both arranged on the common bulk region.

18. (Currently amended) A method of forming a bulk region of a nonvolatile semiconductor device, said method comprising:

forming a bulk region for memory cell transistors provided in a cell array block of the nonvolatile semiconductor memory device, wherein the memory cell transistors of the cell array block is are arranged in an (M x N) array with M and N both at least equal to two; and

forming a bulk region for decoder transistors of a column decoder in the bulk region for the memory cell transistors of the cell array block, wherein the column decoder transistors of the column decoder is are arranged ~~in a (P x N)~~ within a (N x N) array with P at least equal to one adjacent to the cell array block.

19. (Original) A method of forming a bulk region of a nonvolatile semiconductor device, according to claim 18, further comprising configuring the bulk regions for the memory cell transistors and decoder transistors to receive a common bulk signal during an erase operation.

20. (Original) A method of forming a bulk region of a nonvolatile semiconductor device, according to claim 18, wherein said memory cell transistors and said decoder transistors are configured to be simultaneously erased with each other during an erase operation.

21. (Withdrawn) A nonvolatile semiconductor memory device comprising:
a plurality of sectors, wherein each sector further comprises a plurality of memory cell transistors arranged in a (M x N) array having M word lines and N bit lines where M is at least equal to two; wherein each sector further comprises N decoder transistors corresponding

to one of the N bit lines, wherein the plurality of memory cell transistors and the N decoder transistors share a common bulk region, and wherein the semiconductor memory device is configured to electrically erase the plurality of memory cell transistors simultaneously.

22. (Withdrawn) A sector structure of a nonvolatile semiconductor memory, the sector structure comprising:

a plurality of memory cell transistors arranged in a (M x N) array where M is at least equal to two; and

N decoder transistors, wherein the plurality of memory cell transistors and the N decoder transistors are arranged on a common bulk region.

23. (Withdrawn) A nonvolatile semiconductor memory device, comprising:

a (M x N) array, wherein M is at least equal to two, comprising a plurality of memory cell transistors having gates and drains, each gate connected to a corresponding one of M word lines, each drain connected to a corresponding one of N bit lines;

a source line driver commonly connected to a source of each of the plurality of memory cell transistors;

a column decoder comprising N column decoder transistors connected between the N bit lines and a common data line;

a common bulk region, wherein the plurality of memory cell transistors and the N column decoder transistors share the common bulk region; and

a bulk driver configured to commonly apply a bulk voltage to the common bulk region.

24. (Withdrawn) A nonvolatile semiconductor memory device comprising:

a plurality of sector units, each sector unit comprising a common bulk region wherein each sector unit is configured to be electrically erasable in response to an erase signal, wherein each of the plurality of sector units further comprises a (M x N) array of memory cell transistors arranged in the common bulk region of each sector unit and configured to commonly receive a bulk voltage, wherein M is at least equal to two, and wherein each of the plurality of sector units further comprises a (1 x N) array of column decoder transistors arranged in the common bulk region of each sector unit and configured to commonly receive the bulk voltage.

25. (Withdrawn) A method of forming a bulk region of a nonvolatile semiconductor device comprising:

forming a first bulk region for a plurality of memory cell transistors provided in a (M x N) array, wherein M is at least equal to two; and

forming a second bulk region for N column decoder transistors, wherein the first and the second bulk regions are integrally connected.

26. (Currently amended) The device of claim 1, wherein the cell array block and the column decoder block ~~of each sector~~ share a plurality of word lines and a plurality of bit lines.

27. (Currently amended) The device of claim 17, wherein the plurality of memory cell transistors of the cell array block is are arranged in a (M x N) array and the plurality of column decoder transistors of the column decoder block is are arranged ~~in a (P x N)~~ within a (N x N) array adjacent to the cell array block, where M and N are at least equal to two ~~and P is at least equal to one~~.